

SOSAM 1.35V DDR3L SODIMM DATASHEET V1.0

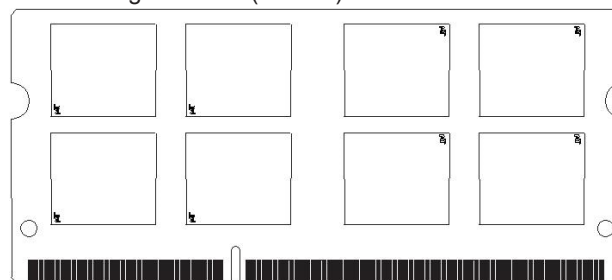
1.35V DDR3L SDRAM SODIMM

Features

- DDR3L functionality and operations supported as defined in the component data sheet
- 204-pin, small outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC3-14900, PC3-12800, or PC3-10600
- 4GB (512 Meg x 64), 8GB (1 Gig x 64)
- $V_{DD} = 1.35V$ (1.283V–1.45V)
- $V_{DD} = 1.5V$ (1.425–1.575V)
- Backward compatible to $V_{DD} = 1.5V \pm 0.075V$
- $V_{DDSPD} = 3.0\text{--}3.6V$
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Dual rank
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- On-board I²C serial presence-detect (SPD) EEPROM
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 204-Pin SODIMM

Module height: 30mm (1.181in)



Options

- Operating temperature
 - Commercial ($0^{\circ}C \leq T_A \leq +70^{\circ}C$)
- Package
 - 204-pin DIMM (halogen-free)
- Frequency/CAS latency
 - 1.07ns @ CL = 13 (DDR3L-1866)
 - 1.25ns @ CL = 11 (DDR3L-1600)
 - 1.5ns @ CL = 9 (DDR3L-1333)

Marking

None

Z

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)								t_{RCD} (ns)	t_{RP} (ns)	t_{RC} (ns)
		CL = 13	CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
	PC3-14900	1866	1600	1333	1333	1066	1066	800	667	13.125	13.125	47.125
	PC3-12800	–	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
	PC3-10600	–	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
	PC3-8500	–	–	–	–	1066	1066	800	667	13.125	13.125	50.625
	PC3-8500	–	–	–	–	1066	–	800	667	15	15	52.5
	PC3-6400	–	–	–	–	–	–	800	667	15	15	52.5

Table 2: Addressing

Parameter	4GB	8GB
Refresh count	8K	8K
Row address	32K A[14:0]	64K A[15:0]
Device bank address	8 BA[2:0]	8 BA[2:0]
Device configuration	2Gb (256 Meg x 8)	4Gb (512 Meg x 8)
Column address	1K A[9:0]	1K A[9:0]
Module rank address	2 S#[1:0]	2 S#[1:0]

Table 3: Part Numbers and Timing Parameters – 4GB / 8GB Modules

Base device: 2Gb / 4Gb 1.35V DDR3L SDRAM

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- t_{RCD} - t_{RP})
KMD3S08GB2M118DC	8GB	1 Gig x 64	14.9 GB/s	1.07ns/1866 MT/s	13-13-13
KMD3S04GB2M116DC KMD3S08GB2M116DC	4GB / 8GB	512 Meg x 64 1 Gig x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
KMD3S04GB2M113DC KMD3S08GB2M113DC	4GB / 8GB	512 Meg x 64 1 Gig x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9

Pin Assignments

Table 5: Pin Assignments

204-Pin VDDR3L SODIMM Front								204-Pin VDDR3L SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	53	DQ19	105	VDD	157	DQ42	2	VSS	54	VSS	106	VDD	158	DQ46
3	VSS	55	VSS	107	A10	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47
5	DQ0	57	DQ24	109	BA0	161	VSS	6	DQ5	58	DQ29	110	RAS#	162	VSS
7	DQ1	59	DQ25	111	VDD	163	DQ48	8	VSS	60	VSS	112	VDD	164	DQ52
9	VSS	61	VSS	113	WE#	165	DQ49	10	DQS0#	62	DQS3#	114	S0#	166	DQ53
11	DM0	63	DM3	115	CAS#	167	VSS	12	DQS0	64	DQS3	116	ODT0	168	VSS
13	VSS	65	VSS	117	VDD	169	DQS6#	14	VSS	66	VSS	118	VDD	170	DM6
15	DQ2	67	DQ26	119	A13	171	DQS6	16	DQ6	68	DQ30	120	ODT1	172	VSS
17	DQ3	69	DQ27	121	S1#	173	VSS	18	DQ7	70	DQ31	122	NC	174	DQ54
19	VSS	71	VSS	123	VDD	175	DQ50	20	VSS	72	VSS	124	VDD	176	DQ55
21	DQ8	73	CKE0	125	NC	177	DQ51	22	DQ12	74	CKE1	126	VREFCA	178	VSS
23	DQ9	75	VDD	127	VSS	179	VSS	24	DQ13	76	VDD	128	VSS	180	DQ60
25	VSS	77	NC	129	DQ32	181	DQ56	26	VSS	78	NC/A15	130	DQ36	182	DQ61
27	DQS1#	79	BA2	131	DQ33	183	DQ57	28	DM1	80	A14	132	DQ37	184	VSS
29	DQS1	81	VDD	133	VSS	185	VSS	30	RESET#	82	VDD	134	VSS	186	DQS7#
31	VSS	83	A12	135	DQS4#	187	DM7	32	VSS	84	A11	136	DM4	188	DQS7
33	DQ10	85	A9	137	DQS4	189	VSS	34	DQ14	86	A7	138	VSS	190	VSS
35	DQ11	87	VDD	139	VSS	191	DQ58	36	DQ15	88	VDD	140	DQ38	192	DQ62
37	VSS	89	A8	141	DQ34	193	DQ59	38	VSS	90	A6	142	DQ39	194	DQ63
39	DQ16	91	A5	143	DQ35	195	VSS	40	DQ20	92	A4	144	VSS	196	VSS
41	DQ17	93	VDD	145	VSS	197	SA0	42	DQ21	94	VDD	146	DQ44	198	NF
43	VSS	95	A3	147	DQ40	199	VDDSPD	44	VSS	96	A2	148	DQ45	200	SDA
45	DQS2#	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	VSS	202	SCL
47	DQS2	99	VDD	151	VSS	203	TT	48	VSS	100	VDD	152	DQS5#	204	VTT
49	VSS	101	CK0	153	DM5	–	–	50	DQ22	102	CK1	154	DQS5	–	–
51	DQ18	103	CK0#	155	VSS	–	–	52	DQ23	104	CK1#	156	VSS	–	–

Note: 1. Pin 78 is NC 4GB, A15 for 8GB.

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3L modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 6: Pin Descriptions

Symbol	Type	Description
Ax	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments table for density-specific addressing information.
BAx	Input	Bank address inputs: Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	Clock: Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	Clock enable: Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	Data mask (x8 devices only): DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	On-die termination: Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3L SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	Parity input: Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	Reset: RESET# is an active LOW asynchronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	Chip select: Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I ² C bus.
SCL	Input	Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I ² C bus.
CBx	I/O	Check bits: Used for system error detection and correction.
DQx	I/O	Data input/output: Bidirectional data bus.
DQSx, DQSx#	I/O	Data strobe: Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

Table 6: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	Serial data: Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I ² C bus.
TDQSx, TDQSx#	Output	Redundant data strobe (x8 devices only): TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	Parity error output: Parity error found on the command and address bus.
EVENT#	Output (open drain)	Temperature event: The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
VDD	Supply	Power supply: 1.35V (1.283–1.45V) backward-compatible to 1.5V (1.425–1.575V). The component VDD and VDDQ are connected to the module VDD.
VDDSPD	Supply	Temperature sensor/SPD EEPROM power supply: 3.0–3.6V.
VREFCA	Supply	Reference voltage: Control, command, and address VDD/2.
VREFDQ	Supply	Reference voltage: DQ, DM VDD/2.
VSS	Supply	Ground.
VTT	Supply	Termination voltage: Used for control, command, and address VDD/2.
NC	–	No connect: These pins are not connected on the module.
NF	–	No function: These pins are connected within the module, but provide no functionality.

DQ Map

Table 7: Component-to-Module DQ Map, PCB 0900 R/C-F (Front)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	2	15	U2	0	18	51
	1	5	6		1	21	42
	2	3	17		2	19	53
	3	0	5		3	16	39
	4	6	16		4	22	50
	5	4	4		5	20	40
	6	7	18		6	23	52
	7	1	7		7	17	41
U5	0	42	157	U6	0	58	191
	1	45	148		1	61	182
	2	43	159		2	59	193
	3	40	147		3	56	181
	4	46	158		4	62	192
	5	44	146		5	60	180
	6	47	160		6	63	194
	7	41	149		7	57	183
U7	0	13	24	U8	0	26	67
	1	10	33		1	29	58
	2	8	21		2	27	69
	3	11	35		3	24	57
	4	9	23		4	30	68
	5	15	36		5	28	56
	6	12	22		6	31	70
	7	14	34		7	25	59
U9	0	34	141	U10	0	53	166
	1	37	132		1	50	175
	2	35	143		2	48	163
	3	32	129		3	51	177
	4	38	140		4	49	165
	5	36	130		5	55	176
	6	39	142		6	52	164
	7	33	131		7	54	174

Table 8: Component-to-Module DQ Map, PCB 0900 R/C-F (Back)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	61	182	U12	0	45	148
	1	58	191		1	42	157
	2	56	181		2	40	147
	3	59	193		3	43	159
	4	57	183		4	41	149
	5	63	194		5	47	160
	6	60	180		6	44	146
	7	62	192		7	46	158
U15	0	21	42	U16	0	5	6
	1	18	51		1	2	15
	2	16	39		2	0	5
	3	19	53		3	3	17
	4	17	41		4	1	7
	5	23	52		5	7	18
	6	20	40		6	4	4
	7	22	50		7	6	16
U17	0	50	175	U18	0	37	132
	1	53	166		1	34	141
	2	51	177		2	32	129
	3	48	163		3	35	143
	4	54	174		4	33	131
	5	52	164		5	39	142
	6	55	176		6	36	130
	7	49	165		7	38	140
U19	0	29	58	U20	0	10	33
	1	26	67		1	13	24
	2	24	57		2	11	35
	3	27	69		3	8	21
	4	25	59		4	14	34
	5	31	70		5	12	22
	6	28	56		6	15	36
	7	30	68		7	9	23

Table 9: Component-to-Module DQ Map, PCB 1569 R/C-F3 (Front)

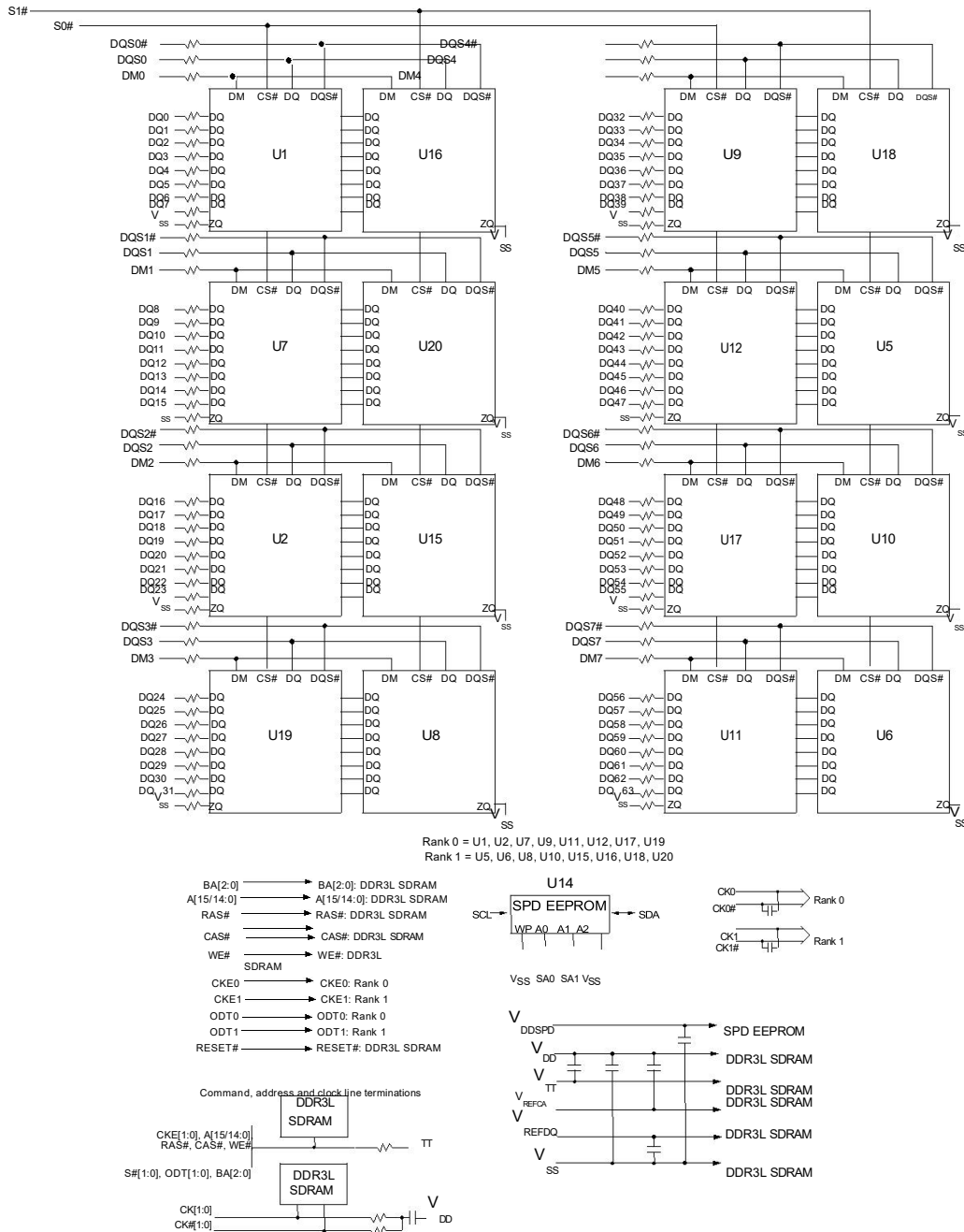
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U2	0	2	13	U3	0	18	49
	1	5	6		1	21	42
	2	3	15		2	19	51
	3	0	5		3	16	37
	4	6	16		4	22	48
	5	4	4		5	20	40
	6	7	18		6	23	50
	7	1	7		7	17	39
U4	0	42	159	U5	0	58	191
	1	45	150		1	61	182
	2	43	161		2	59	193
	3	40	151		3	56	183
	4	46	160		4	62	192
	5	44	148		5	60	180
	6	47	162		6	63	194
	7	41	153		7	57	185
U6	0	13	24	U7	0	26	63
	1	10	31		1	29	56
	2	8	19		2	27	65
	3	11	33		3	24	55
	4	9	21		4	30	66
	5	15	36		5	28	54
	6	12	22		6	31	68
	7	14	34		7	25	57
U8	0	34	145	U9	0	53	168
	1	37	136		1	50	177
	2	35	147		2	48	165
	3	32	133		3	51	179
	4	38	142		4	49	167
	5	36	134		5	55	176
	6	39	144		6	52	166
	7	33	135		7	54	174

Table 10: Component-to-Module DQ Map, PCB 1569 R/C-F (Back)

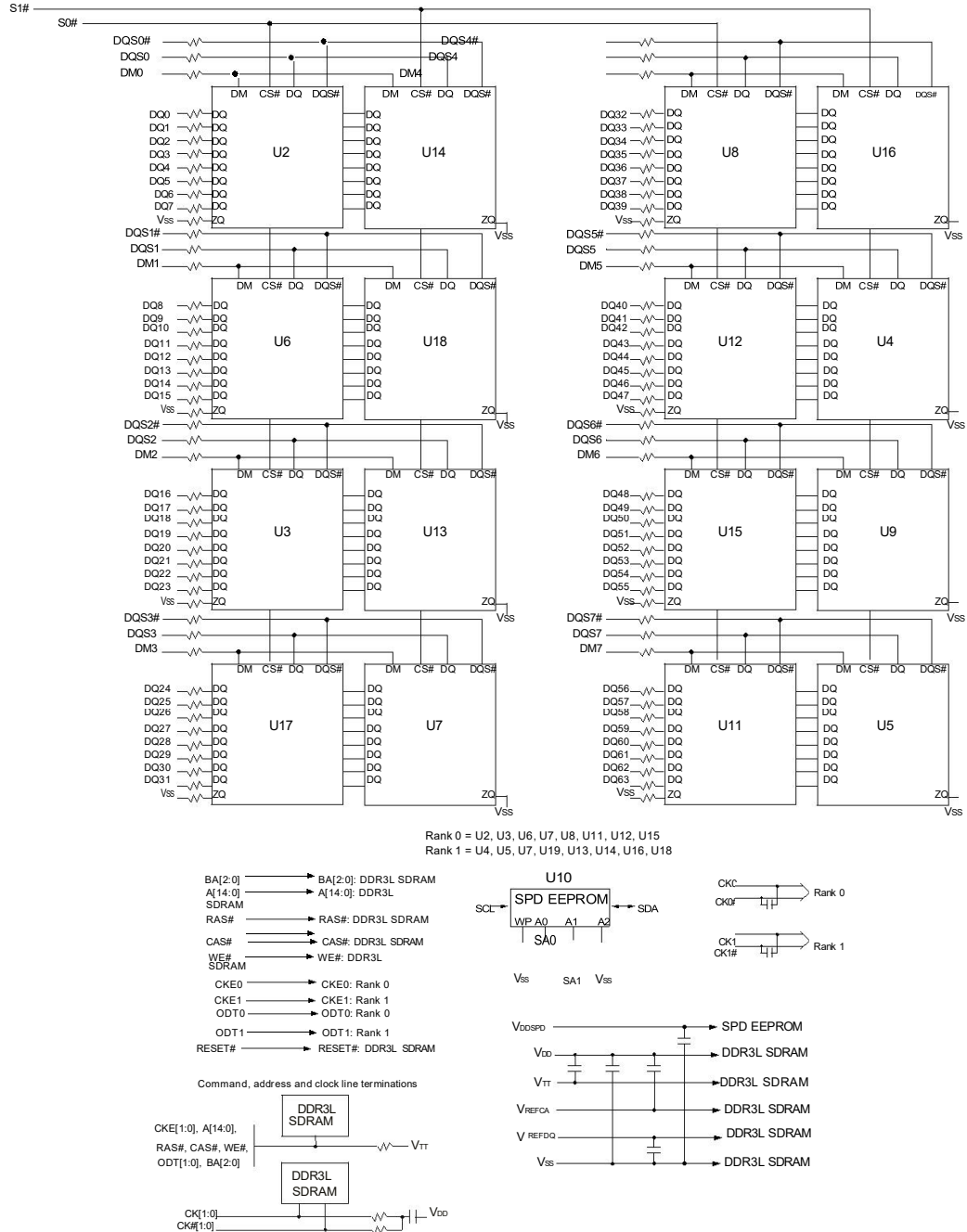
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	61	182	U12	0	45	150
	1	58	191		1	42	159
	2	56	183		2	40	151
	3	59	193		3	43	161
	4	57	185		4	41	153
	5	63	194		5	47	162
	6	60	180		6	44	148
	7	62	192		7	46	160
U13	0	21	42	U14	0	5	6
	1	18	49		1	2	13
	2	16	37		2	0	5
	3	19	51		3	3	15
	4	17	39		4	1	7
	5	23	50		5	7	18
	6	20	40		6	4	4
	7	22	48		7	6	16
U15	0	50	177	U16	0	37	136
	1	53	168		1	34	145
	2	51	179		2	32	133
	3	48	165		3	35	147
	4	54	174		4	33	135
	5	52	166		5	39	144
	6	55	176		6	36	134
	7	49	167		7	38	142
U17	0	29	56	U18	0	10	31
	1	26	63		1	13	24
	2	24	55		2	11	33
	3	27	65		3	8	19
	4	25	57		4	14	34
	5	31	68		5	12	22
	6	28	54		6	15	36
	7	30	66		7	9	21

Functional Block Diagram

Figure 2: Functional Block Diagram (PCB 0900, R/C-F)



Note: 1. The ZQ ball on each DDR3L component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Figure 3: Functional Block Diagram (PCB 1569, R/C-F3)


Note: 1. The ZQ ball on each DDR3L component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

DDR3L SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3L SDRAM devices. DDR3L SDRAM modules use DDR architecture to achieve high-speed operation. DDR3L architecture is essentially an $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3L SDRAM module effectively consists of a single $8n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3L modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3L modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3L.

Serial Presence-Detect EEPROM Operation

DDR3L SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3L SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 11: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V _{DD}	V _{DD} supply voltage relative to V _{SS}	-0.4	1.975	V
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.4	1.975	V

Table 12: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V _{DD}	V _{DD} supply voltage		1.283	1.35	1.45	V	
			1.425	1.5	1.575	V	1
I _{VTT}	Termination reference current from V _{TT}		−600	−	600	mA	
V _{TT}	Termination reference voltage (DC) – command/address bus		0.49 × V _{DD} - 20mV	0.5 × V _{DD}	0.51 × V _{DD} + 20mV	V	2
I _I	Input leakage current; Any input 0V ≤ V _{IN} ≤ V _{DD} ; V _{REF} input 0V ≤ V _{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA	−32	0	32	μA	
		S#, CKE, ODT, CK, CK#	−16	0	16		
		DM	−4	0	4		
I _{oz}	Output leakage current; 0V ≤ V _{OUT} ≤ V _{DD} ; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	−10	0	10	μA	
I _{VREF}	V _{REF} supply leakage current; $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)		−16	0	16	μA	
T _A	Module ambient operating temperature	Commercial	0	−	70	°C	3, 4
T _C	DDR3L SDRAM component case operating temperature	Commercial	0	−	95	°C	3, 4, 5

Notes: 1. Module is backward-compatible with 1.5V operation. Refer to device specification for details and operation guidance.

2. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.

3. T_A and T_C are simultaneous requirements.

4. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3L component data sheets. Module speed grades correlate with component speed grades, as shown below.

Table 13: Module and Component Speed Grades

DDR3L components may exceed the listed module speed grades; module may not be available in all listed speed grades

Design Considerations

Simulations

Memory modules are designed to optimize signal integrity through carefully de-signed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. Of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to en-sure the required supply voltage is maintained.

I_{DD} Specifications

Table 14: DDR3L I_{DD} Specifications and Conditions – 4GB (Die Revision K)

Values are for the DDR3L SDRAM only and are computed from values specified in the 1.35V 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	¹ I _{DD0}	408	400	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	¹ I _{DD1}	512	496	mA
Precharge power-down current: Slow exit	² I _{DD2P0}	192	192	mA
Precharge power-down current: Fast exit	² I _{DD2P1}	224	224	mA
Precharge quiet standby current	² I _{DD2Q}	320	320	mA
Precharge standby current	² I _{DD2N}	336	336	mA
Precharge standby ODT current	¹ I _{DD2NT}	344	328	mA
Active power-down current	² I _{DD3P}	336	336	mA
Active standby current	² I _{DD3N}	512	480	mA
Burst read operating current	¹ I _{DD4R}	848	752	mA
Burst write operating current	¹ I _{DD4W}	872	776	mA
Refresh current	¹ I _{DD5B}	1536	1528	mA
Self refresh temperature current: MAX T _C = 85°C	² I _{DD6}	192	192	mA
Self refresh temperature current (SRT-enabled): MAX T _C = 95°C	² I _{DD6ET}	240	240	mA
All banks interleaved read current	¹ I _{DD7}	1344	1296	mA
Reset current	² I _{DD8}	224	224	mA

Notes: 1. One module rank in the active I_{DD}; the other rank in I_{DD2P0} (slow exit).

2. All ranks in this I_{DD} condition.

Table 15: DDR3L I_{DD} Specifications and Conditions – 8GB (Die Revisions E)

Values are for the DDR3L SDRAM only and are computed from values specified in the 1.35V 4Gb (512 Meg x 8) component data sheet

Parameter	Symbol	1866	1600	1333	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	¹ I _{DD0}	640	584	520	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	¹ I _{DD1}	704	672	640	mA
Precharge power-down current: Slow exit	² I _{DD2P0}	288	288	288	mA
Precharge power-down current: Fast exit	² I _{DD2P1}	592	512	448	mA
Precharge quiet standby current	² I _{DD2Q}	560	512	448	mA
Precharge standby current	² I _{DD2N}	560	512	464	mA
Precharge standby ODT current	¹ I _{DD2NT}	480	456	424	mA
Active power-down current	² I _{DD3P}	656	608	560	mA
Active standby current	² I _{DD3N}	656	608	560	mA
Burst read operating current	¹ I _{DD4R}	1536	1400	1264	mA
Burst write operating current	¹ I _{DD4W}	1272	1144	1024	mA
Refresh current	¹ I _{DD5B}	2080	2024	1968	mA
Self refresh temperature current: MAX T _C = 85°C	² I _{DD6}	320	320	320	mA
Self refresh temperature current (SRT-enabled): MAX T _C = 95°C	² I _{DD6ET}	400	400	400	mA
All banks interleaved read current	¹ I _{DD7}	2152	1904	1664	mA
Reset current	² I _{DD8}	320	320	320	mA

Notes: 1. One module rank in the active I_{DD}; the other rank in I_{DD2P0} (slow exit).

2. All ranks in this I_{DD} condition.

Table 16: DDR3L I_{DD} Specifications and Conditions – 8GB (Die Revision N)

Values are for the DDR3L SDRAM only and are computed from values specified in the 1.35V 4Gb (512 Meg x 8) component data sheet

Parameter	Symbol	1866	1600	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	¹ I _{DD0}	456	440	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	¹ I _{DD1}	576	552	mA
Precharge power-down current: Slow exit	² I _{DD2P0}	128	128	mA
Precharge power-down current: Fast exit	² I _{DD2P1}	256	224	mA
Precharge quiet standby current	² I _{DD2Q}	416	384	mA
Precharge standby current	² I _{DD2N}	416	384	mA
Precharge standby ODT current	¹ I _{DD2NT}	304	288	mA
Active power-down current	² I _{DD3P}	448	416	mA
Active standby current	² I _{DD3N}	512	480	mA
Burst read operating current	¹ I _{DD4R}	904	824	mA
Burst write operating current	¹ I _{DD4W}	904	824	mA
Refresh current	¹ I _{DD5B}	1504	1464	mA
Self refresh temperature current: MAX T _C = 85°C	² I _{DD6}	192	192	mA
Self refresh temperature current (SRT-enabled): MAX T _C = 95°C	² I _{DD6ET}	256	256	mA
All banks interleaved read current	¹ I _{DD7}	1184	1104	mA
Reset current	² I _{DD8}	160	160	mA

Notes: 1. One module rank in the active I_{DD}; the other rank in I_{DD2P0} (slow exit).

2. All ranks in this I_{DD} condition.

Table 17: DDR3L I_{DD} Specifications and Conditions – 8GB (Die Revision P)

Values are for the DDR3L SDRAM only and are computed from values specified in the 1.35V 4Gb (512 Meg x 8) component data sheet

Parameter	Symbol	1866	1600	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	¹ I _{DD0}	320	304	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	¹ I _{DD1}	440	424	mA
Precharge power-down current: Slow exit	² I _{DD2P0}	176	160	mA
Precharge power-down current: Fast exit	² I _{DD2P1}	176	176	mA
Precharge quiet standby current	² I _{DD2Q}	240	240	mA
Precharge standby current	² I _{DD2N}	272	256	mA
Precharge standby ODT current	¹ I _{DD2NT}	264	240	mA
Active power-down current	² I _{DD3P}	240	240	mA
Active standby current	² I _{DD3N}	336	320	mA
Burst read operating current	¹ I _{DD4R}	904	800	mA
Burst write operating current	¹ I _{DD4W}	992	888	mA
Refresh current	¹ I _{DD5B}	1304	1296	mA
Self refresh temperature current: MAX T _C = 85°C	² I _{DD6}	240	240	mA
Self refresh temperature current (SRT-enabled): MAX T _C = 95°C	² I _{DD6ET}	368	368	mA
All banks interleaved read current	¹ I _{DD7}	1256	1120	mA
Reset current	² I _{DD8}	208	208	mA

Notes: 1. One module rank in the active I_{DD}; the other rank in I_{DD2P0} (slow exit).

2. All ranks in this I_{DD} condition.

Serial Presence-Detect EEPROM

Table 18: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{DDSPD}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V _{DDSPD}	3.0	3.6	V
Input low voltage: Logic 0; All inputs	V _{IL}	-0.45	V _{DDSPD} × 0.3	V
Input high voltage: Logic 1; All inputs	V _{IH}	V _{DDSPD} × 0.7	V _{DDSPD}	V
Output low voltage: I _{OUT} = 3mA	V _{OL}	–	0.4	V
Input leakage current: V _{IN} = GND to V _{DD}	I _{LI}	0.1	2.0	μA
Output leakage current: V _{OUT} = GND to V _{DD}	I _{LO}	0.05	2.0	μA

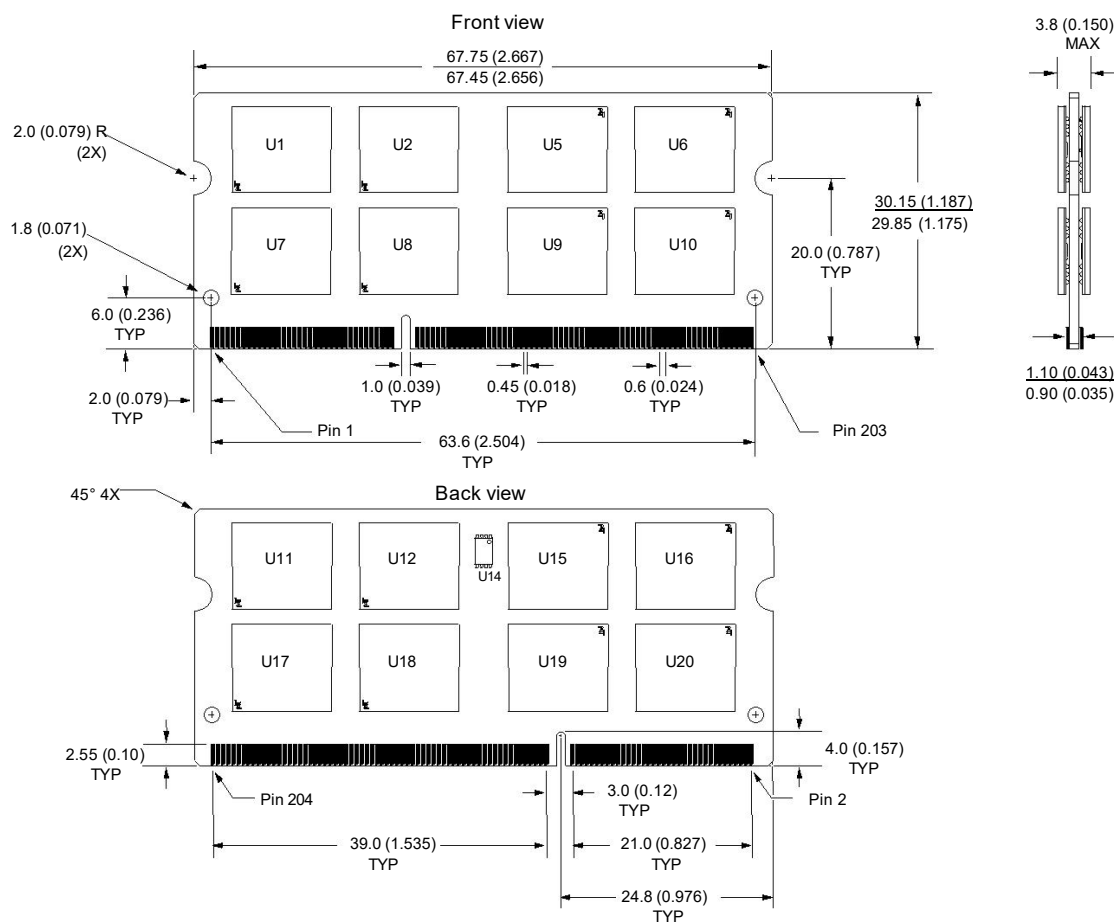
Table 19: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock frequency	t _{SCL}	10	400	kHz	
Clock pulse width HIGH time	t _{HIGH}	0.6	–	μs	
Clock pulse width LOW time	t _{LOW}	1.3	–	μs	
SDA rise time	t _R	–	300	μs	1
SDA fall time	t _F	20	300	ns	1
Data-in setup time	t _{SU:DAT}	100	–	ns	
Data-in hold time	t _{HD:DI}	0	–	μs	
Data-out hold time	t _{HD:DAT}	200	900	ns	
Data out access time from SCL LOW	t _{AA:DAT}	0.2	0.9	μs	2
Start condition setup time	t _{SU:STA}	0.6	–	μs	3
Start condition hold time	t _{HD:STA}	0.6	–	μs	
Stop condition setup time	t _{SU:STO}	0.6	–	μs	
Time the bus must be free before a new transition can start	t _{BUF}	1.3	–	μs	
WRITE time	t _W	–	10	ms	

- Notes:
1. Guaranteed by design and characterization, not necessarily tested.
 2. To avoid spurious start and stop conditions, a minimum delay is placed between the fall-ing edge of SCL and the falling or rising edge of SDA.
 3. For a restart condition, or following a WRITE cycle.

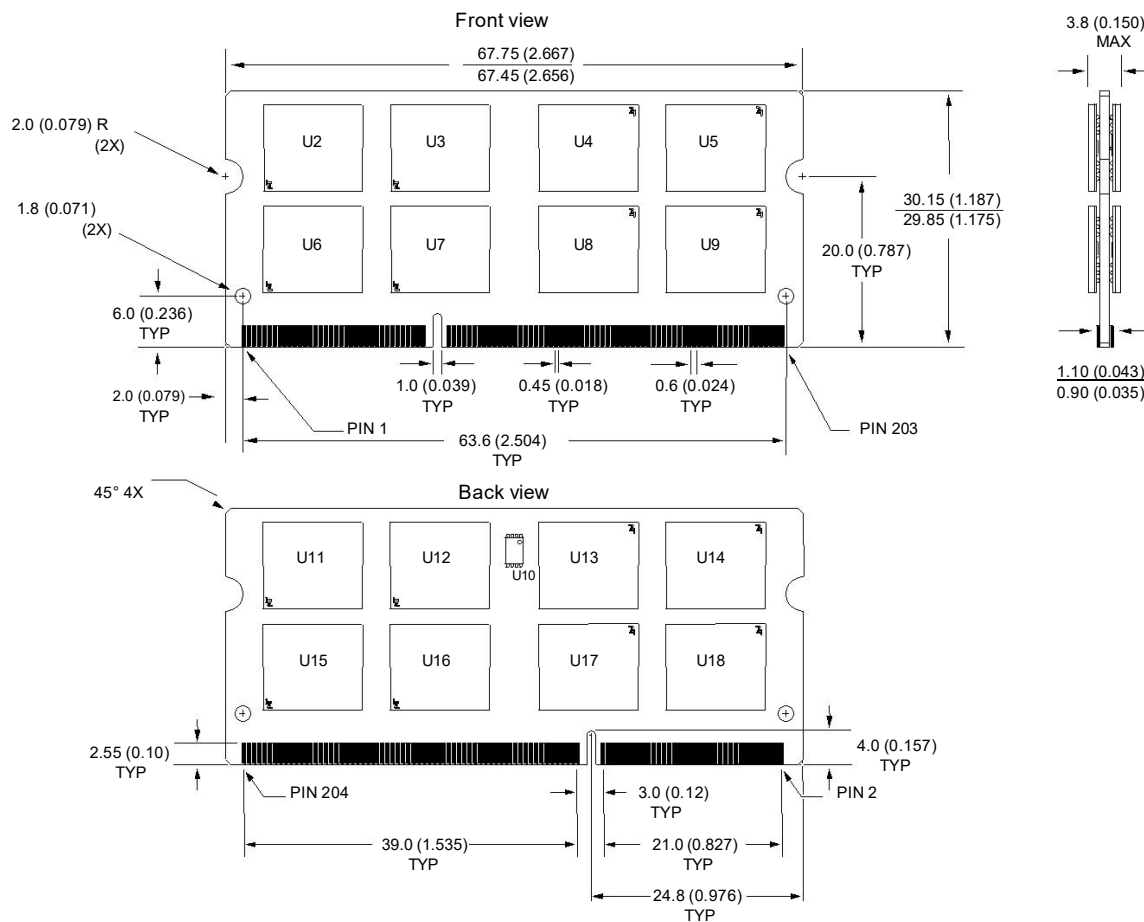
Module Dimensions

Figure 4: 204-Pin DDR3L SODIMM (PCB 0900, R/C-F)



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only.

Figure 5: 204-Pin DDR3L SODIMM (PCB 1569, R/C-F3)



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

For More Information

For Technical Support:

If additional support is needed, please visit the SOSAM Web site at www.kumi2020.com

for the following topics:

- **Warranty Services:** Includes the warranty service policy and the RMA request forms.
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- **Tools Section:** Includes frequently asked questions (FAQs).

For More Information or Further Technical Support Please Contact:

Shenzhen Kumi industry co. LTD

Tel: +86 13620595629

Support: zhuchunhong@kumi2020.com