

SOSAM DDR4 SODIMM 8GB 3200 Datasheet Ver1.0

I.Product Basic Information

- Memory Type: PC4-25600 Unbuffered Non-ECC 260pin DDR4 SODIMM
- Memory Model: DDR4-3200 VDD-1.2V
- Memory Capacity: 8GB
- IC Model: DDR4-1Gbx8

II.Technical Specifications

2.1 Memory Parameters

Item	Data
Part Number	KMD4S08GC1M632DC
Working leadtime	DDR4-3200 CL=22 $t_{\text{rcd}}=22$, $t_{\text{rp}}=22$
Capacity	8GB
Chipset model#	D9VPP
Chipset structure	1Gbx8
Chipset quantity	8PCS
SPD	Yes
ECC	No
BUFFER	No

2.2 Environmental Requirements

Item	Data
Working temperature	0°C~+85°C
Working Humidity	10%—90%
Storage temperature	-50°C~+100°C
Storage Humidity	5%—95%
Working Storage Atmospheric Pressure	69—105KPa

2.3 SPD Description

SPD Must Meet JESD "DDR4 SPD Document Release 4" standard.

2.4 PCB Performance Parameters

Item	Data
Golden pin	260 pin
PCB Size(mm * mm)	69.60* 30.00±0.1mm
Impedance	Single-ended 50/55Ω±10% 57Ω±15% Differential 83/93Ω±15%
PCB Layers	8

2.5 Label Description

Label Type	Specification
PCB Board Label	PCB model printed on the board.
Memory Module Label	The memory module label should indicate the main parameters.

III. Electrical parameters

Electrical parameters meet SSTL_1.8 standard.

3.1 Supply Voltage And DC

Parameters	Min (V)	Max (V)
V_{DD} (Supply Voltage)	1.14	1.26
V_{DDQ} (I/O Supply Voltage)	1.14	1.26
V_{REF} (I/O Reference Voltage)	$0.49 \times VDD$	$0.51 \times VDD$
V_{DDSPD} (EEPROM Supply Voltage)	2.25	3.6
$V_{IH}(DC)$ (Input High (Logic 1) Voltage)	$V_{REF} + 0.100$	---
$V_{IL}(DC)$ (Input Low (Logic 0) Voltage)	---	$V_{REF} - 0.100$

3.2 AC Parameters

Parameters	Min (V)	Max (V)
$V_{IH}(AC)$ Input High (Logic 1) Voltage	$V_{REF} + 0.175$	-
$V_{IL}(AC)$ Input Low (Logic 0) Voltage	-	$V_{REF} - 0.175$

AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating (Min.)	Rating (Typ.)	Rating (Max.)	Unit	NOTE
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V	3

NOTE:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

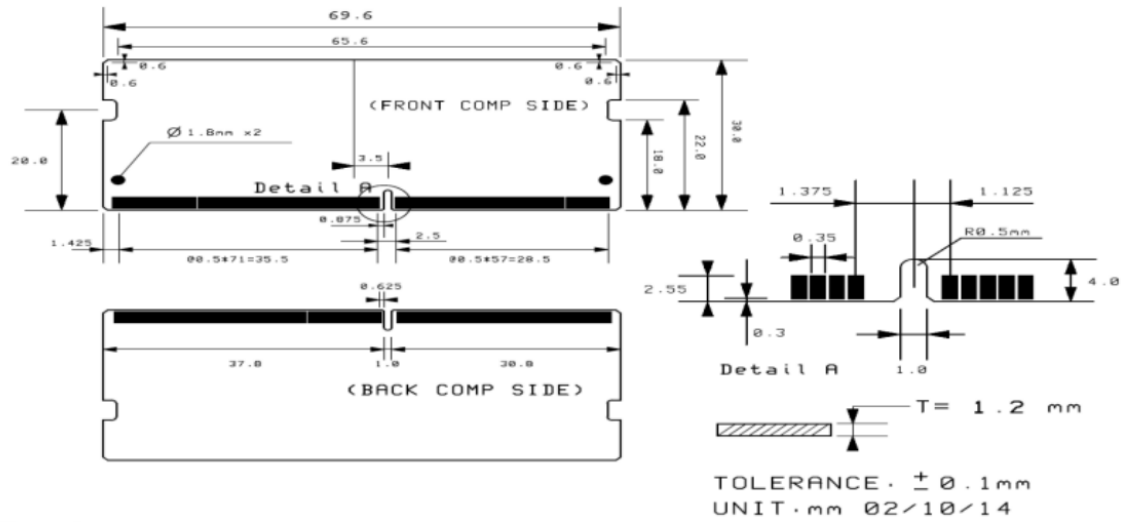
IV. Timing Parameters

DDR4-3200 Speed Bins and Operations

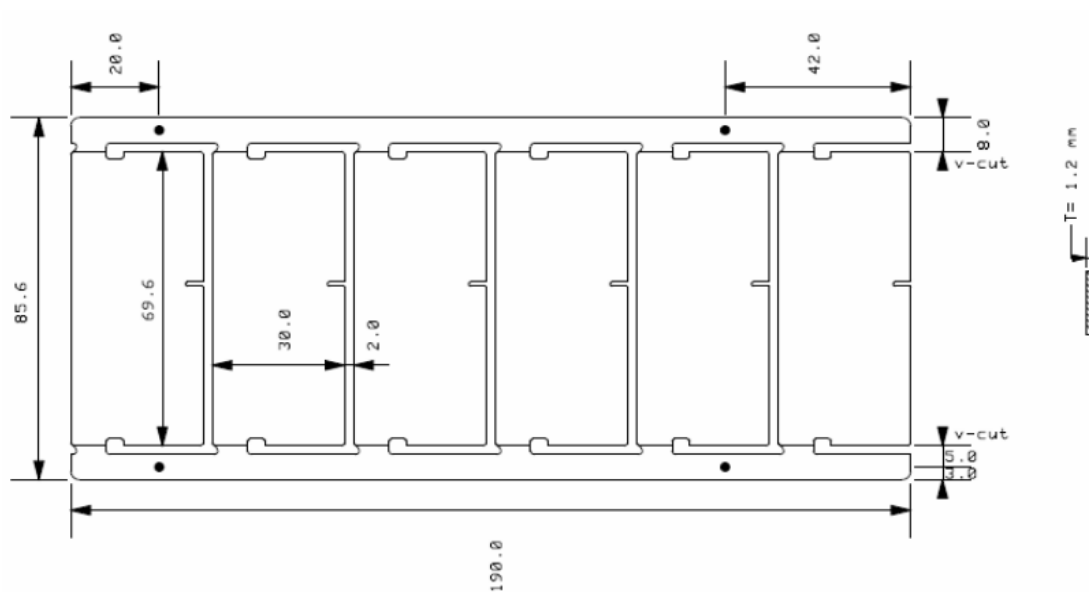
Speed Bin			DDR4-3200AA		Unit	NOTE
CL-nRCD-nRP			22-22-22			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	13.75	18.00	ns	12
Internal read command to first data with read DBI enabled		tAA_DBI	tAA(min) + 4nCK	tAA(max) + 4nCK	ns	12
ACT to internal read or write delay time		tRCD	13.75	-	ns	12
PRE command period		tRP	13.75	-	ns	12
ACT to PRE command period		tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period		tRC	45.75	-	ns	12
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	<1.5	ns	1,2,3,4,10
	CL = 12	CL = 14	tCK(AVG)	<1.5	ns	1,2,3,10
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved	ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	<1.25	ns	1,2,3,4,10
	CL = 14	CL = 16	tCK(AVG)	<1.25	ns	1,2,3,10
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved	ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	<1.071	ns	1,2,3,4,10
	CL = 16	CL = 19	tCK(AVG)	<1.071	ns	1,2,3,10
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved	ns	1,2,3,4,10
	CL = 17	CL = 20	tCK(AVG)	<0.937	ns	1,2,3,4,10
	CL = 18	CL = 21	tCK(AVG)	<0.937	ns	1,2,3,10
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved	ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved	ns	1,2,3,4,10
	CL = 19	CL = 22	tCK(AVG)	<0.833	ns	1,2,3,4,10
	CL = 20	CL = 23	tCK(AVG)	<0.833	ns	1,2,3,10
CWL = 16,20	CL = 20	CL = 24	tCK(AVG)	Reserved	ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)	<0.75	ns	1,2,3,4
	CL = 24	CL = 28	tCK(AVG)	<0.75	ns	1,2,3
Supported CL Settings			10,11,12,13,14,15, 16,17,18,19,20,22, 24		nCK	13
Supported CL Settings with read DBI			12,13,14,15,16,18, 19,20,21,22,23,24, 26, 28		nCK	
Supported CWL Settings			9,10,11,12,14,16, 18,20		nCK	

V.PCB Outlines

Single:



Panel:

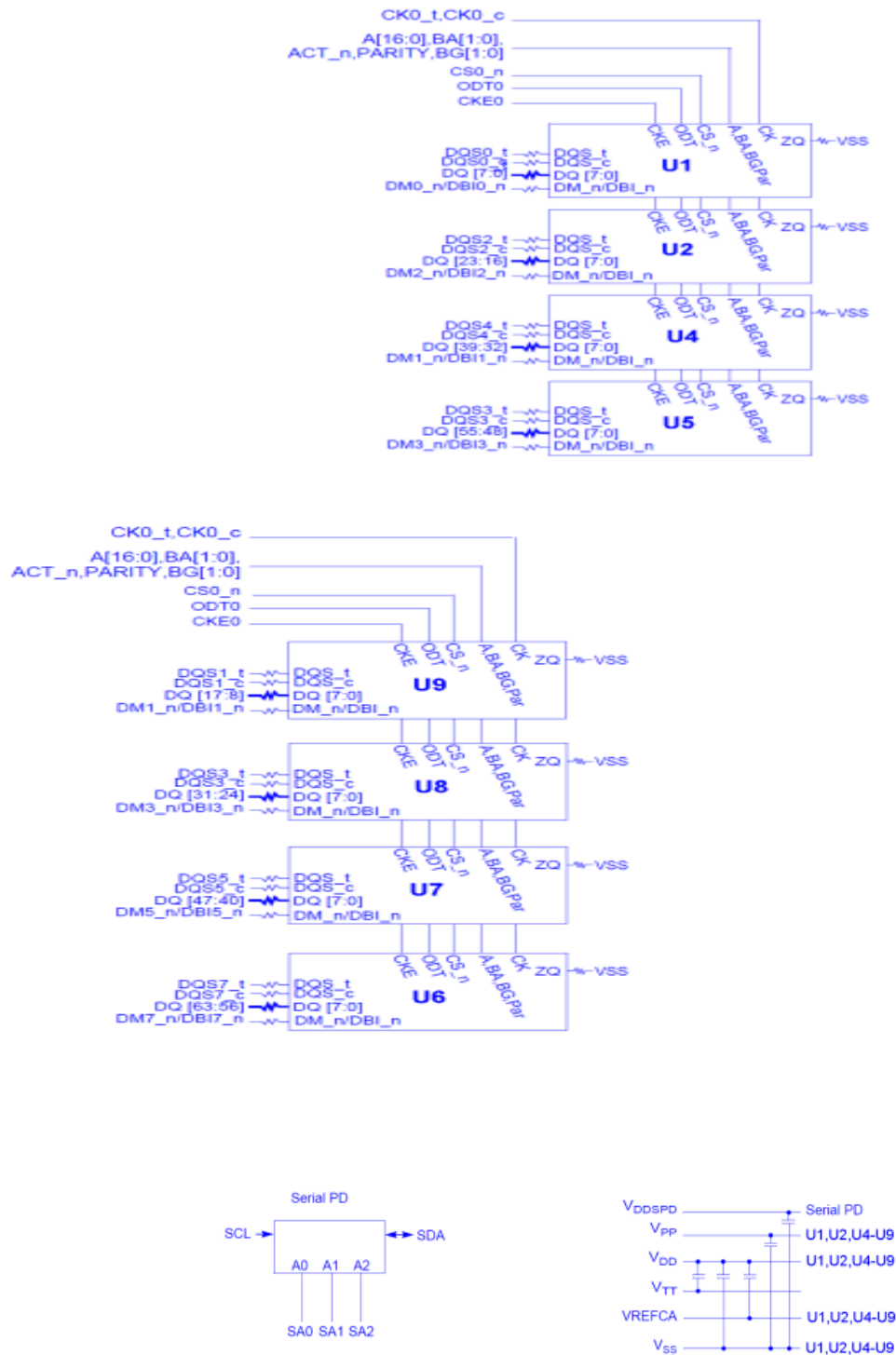


VI.Pin Assignments

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
1	VSS	2	VSS	131	A3	132	A2
3	DQ5	4	DQ4	133	A1	134	EVENT_n
5	VSS	6	VSS	135	VDD	136	VDD
7	DQ1	8	DQ0	137	CK0_t	138	CK1_t
9	VSS	10	VSS	139	CK0_c	140	CK1_c
11	DQ50_c	12	DM0_n, DBI0_n	141	VDD	142	VDD
13	DQ50_t	14	VSS	143	PARITY	144	A0
15	VSS	16	DQ6	KEY			
17	DQ7	18	VSS				
19	VSS	20	DQ2	145	BA1	146	A10/AP
21	DQ3	22	VSS	147	VDD	148	VDD
23	VSS	24	DQ12	149	CS0_n	150	BA0
25	DQ13	26	VSS	151	A14/WE_n	152	A16/RAS_n
27	VSS	28	DQ8	153	VDD	154	VDD
29	DQ9	30	VSS	155	ODT0	156	A15/CAS_n
31	VSS	32	DQ51_c	157	CS1_n	158	A13
33	DM1_n, DBI1_n	34	DQ51_t	159	VDD	160	VDD
35	VSS	36	VSS	161	ODT1	162	CO, CS2_n, NC
37	DQ15	38	DQ14	163	VDD	164	VREFCA
39	VSS	40	VSS	165	Cl, CS3_n, NC	166	SA2
41	DQ10	42	DQ11	167	VSS	168	VSS
43	VSS	44	VSS	169	DQ37	170	DQ36
45	DQ21	46	DQ20	171	VSS	172	VSS
47	VSS	48	VSS	173	DQ33	174	DQ32
49	DQ17	50	DQ16	175	VSS	176	VSS
51	VSS	52	VSS	177	DQ54_c	178	DM4_n, DBI4_n
53	DQ52_c	54	DM2_n, DBI2_n	179	DQ54_t	180	VSS
55	DQ52_t	56	VSS	181	VSS	182	DQ39
57	VSS	58	DQ22	183	DQ38	184	VSS
59	DQ23	60	VSS	185	VSS	186	DQ35
61	VSS	62	DQ18	187	DQ34	188	VSS
63	DQ19	64	VSS	189	VSS	190	DQ45
65	VSS	66	DQ28	191	DQ44	192	VSS
67	DQ29	68	VSS	193	VSS	194	DQ41
69	VSS	70	DQ24	195	DQ40	196	VSS
71	DQ25	72	VSS	197	VSS	198	DQ55_c
73	VSS	74	DQ53_c	199	DM5_n, DBI5_n	200	DQ55_t
75	DM3_n, DBI3_n	76	DQ53_t	201	VSS	202	VSS

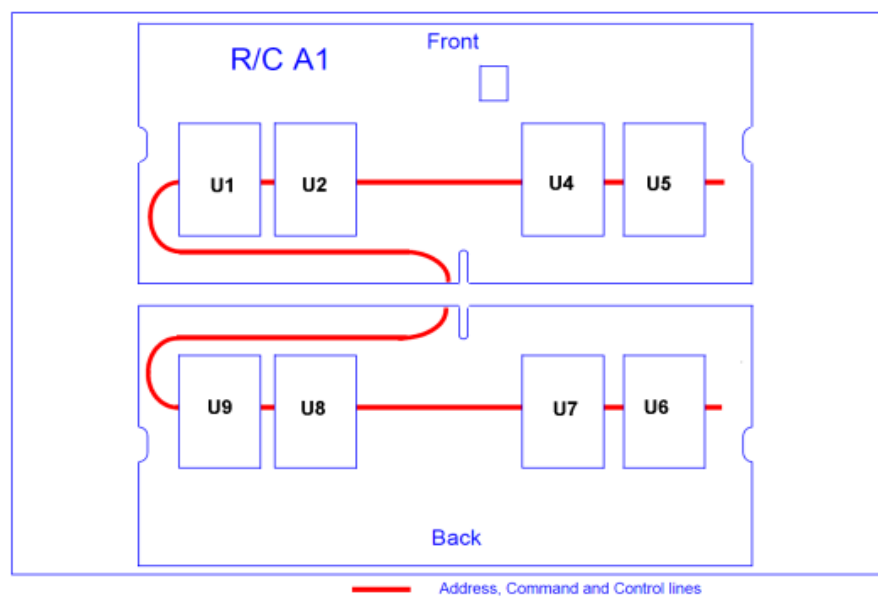
Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
77	VSS	78	VSS	203	DQ46	204	DQ47
79	DQ30	80	DQ31	205	VSS	206	VSS
81	VSS	82	VSS	207	DQ42	208	DQ43
83	DQ26	84	DQ27	209	VSS	210	VSS
85	VSS	86	VSS	211	DQ52	212	DQ53
87	CB5, NC	88	CB4, NC	213	VSS	214	VSS
89	VSS	90	VSS	215	DQ49	216	DQ48
91	CB1, NC	92	CB0, NC	217	VSS	218	VSS
93	VSS	94	VSS	219	DQ56_c	220	DM6_n, DBI6_n
95	DQ58_c	96	DM8_n, DBI8_n	221	DQ56_t	222	VSS
97	DQ58_t	98	VSS	223	VSS	224	DQ54
99	VSS	100	CB6, NC	225	DQ55	226	VSS
101	CB2, NC	102	VSS	227	VSS	228	DQ50
103	VSS	104	CB7, NC	229	DQ51	230	VSS
105	CB3, NC	106	VSS	231	VSS	232	DQ60
107	VSS	108	RESET_n	233	DQ61	234	VSS
109	CKE0	110	CKE1	235	VSS	236	DQ57
111	VDD	112	VDD	237	DQ56	238	VSS
113	BG1	114	ACT_n	239	VSS	240	DQ57_c
115	BG0	116	ALERT_n	241	DM7_n, DBI7_n	242	DQ57_t
117	VDD	118	VDD	243	VSS	244	VSS
119	A12	120	A11	245	DQ62	246	DQ63
121	A9	122	A7	247	VSS	248	VSS
123	VDD	124	VDD	249	DQ58	250	DQ59
125	A8	126	A5	251	VSS	252	VSS
127	A6	128	A4	253	SCL	254	SDA
129	VDD	130	VDD	255	VDDSPD	256	SA0
				257	VPP	258	VTT
				259	VPP	260	SA1

VII.Functional Diagram



Note 1: Unless otherwise noted, resistor values are $15\ \Omega \pm 5\%$.

Note 2: ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.



For More Information

For Technical Support:

If additional support is needed, please visit the SOSAM Web site at www.kumi2020.com

for the following topics:

- **Warranty Services:** Includes the warranty service policy and the RMA requestforms.
- **Technical Information:** Includes product data sheets and various USB whitepapers.
- **Tools Section:** Includes frequently asked questions (FAQs).